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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	09/752,796	YOAZ ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000 and 14 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☒ Claim(s) *20 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-26 have been examined.

Papers Received

2. Receipt is acknowledged of Declaration and Information Disclosure Statement papers submitted, where the papers have been placed of record in the file.

Specification

3. The disclosure is objected to because of the following informalities: the specification does not contain a summary of the invention. See MPEP § 1.73.

4. The disclosure is objected to because of the following informalities: Page 5, line 25 has spelling mistake on the first instance of the word "respective". Also, it is unclear why the distance of a store instruction from another store instruction shown on page 7, lines 5-8, would have any bearing on a silent prediction.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Prediction of Issued Silent Store Operations for Allowing Subsequently Issued Loads to Bypass Unexecuted Silent Stores and Confirming the Bypass Upon Execution of the Stores.

Appropriate correction is required.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the marking,

comparing, and recovery units must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: element 100 of figure 1 is not shown. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: elements 1110, 1130, 1140, and 1150 of figure 11. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

9. Claims 20 and 24 are objected to because of the following informalities: The context of the claim makes it seem as though the marking step is performed after load is prepared for retirement even though the examiner understands that this step is performed after a store is matched with a load and this marking is only checked after the load is prepared as described in the specification and figures. The examiner is

taking the claim to refer to two separate events that are not directly correlated with each other. Clarification is requested on this matter.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 19-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claim 19 recites the limitation "an extended load buffer" in line 1 of page 19. There is insufficient antecedent basis for this limitation in the claim. An extended load buffer was already previously defined in the claim and thus it cannot be determined if that buffer or a new one is being referred to. The examiner is taking the claim to mean "the extended load buffer" in order to refer to the instance already defined and to keep consistent with the specification.

13. Claim 20 recites the limitation "the load instruction flush" in line 8. There is insufficient antecedent basis for this limitation in the claim. The extended buffer to this point has not been defined to include a load instruction flush field. The examiner is taking the claim to mean "a load instruction flush".

14. Claim 23 recites the limitation " an extended load buffer " in line 21 of page 19. There is insufficient antecedent basis for this limitation in the claim. An extended load buffer was already previously defined in the claim and thus it cannot be determined if

that buffer or a new one is being referred to. The examiner is taking the claim to mean "the extended load buffer" in order to refer to the instance already defined and to keep consistent with the specification.

15. Claim 24 recites the limitation "the load operation flush" in line 7. There is insufficient antecedent basis for this limitation in the claim. The extended buffer to this point has not been defined to include a load instruction flush field. The examiner is taking the claim to mean "a load instruction flush".

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1, 6-10, and 15-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle (5,467,473) in view of Yoaz (5,987,595).

18. In regard to claim 1,

a. Kahle discloses an apparatus comprising:

i. an extended load buffer; Figure 5 gives a layout of a load queue which is also a buffer.

ii. a marking unit coupled to the extended load buffer; Figure 6, shows in step 4 that a load program number is placed or marked into the load queue (extended load buffer). Therefore a marking unit must exist to perform this marking.

iii. a comparing unit coupled to the extended load buffer; Figure 6, step 6 and column 2, lines 56-59 show that a store address is compared to the load addresses of the load buffer. For this comparison to take place a comparison unit must exist.

iv. and a recovery unit coupled to the extended load buffer; Figure 6, steps 9 and 10 and column 3, lines 4-11 show that a load instruction must be placed in original order and reexecuted. It is shown that this is because of a conflict that exists and therefore original order must be recovered. This must be accomplished with a recovery unit.

v. wherein unexecuted load instructions are advanced over silent store instructions. Column 2, lines 56-59 show that load instructions are executed out of order ahead of a store. Since load instructions can be advanced past any store, they will also be advanced past silent stores.

b. Kahle does not disclose a predictor having a collision history table (CHT) and that the extended load buffer is coupled to the predictor.

c. Yoaz has disclosed a predictor having a collision history table (CHT) (figure 3, element 88). Column 3, lines 50-52 show that the CHT is used for predicting and thus is part a predictor along with the control unit (figure 3, element 102). Figure 3 shows that the CHT or predictor is coupled to a recorder buffer, 94, using some control logic. Column 6, lines 35-36, shows that this buffer holds entries for load instructions. Yoaz has disclosed in column 3, lines

50-60 that the predictor is used for predicting load instructions so that loads can be executed ahead of stores.

d. Yoaz has shown in column 2, lines 58-63 that his method is able to execute more load instructions out of order (based on the predictor) for faster processor operations. These faster processor operations would have motivated one of ordinary skill in the art to modify the design of Kahle to use the collision history table and predictor described by Yoaz.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Kahle to include the predictor disclosed by Yoaz so that processor operations may be sped up.

19. In regard to claim 6, Kahle in view of Yoaz has disclosed the apparatus of claim 1, as described above, wherein the predictor is memory dependent. Column 3, lines 54-60 of Yoaz show that predictor is based on memory addresses and thus is memory dependant.

20. In regard to claim 7, Kahle in view of Yoaz has disclosed the apparatus of claim 1, wherein the extended load buffer comprises bit fields to mark load address match, load data match, load predict, and load flush, and bit fields for load address, load attribute and load data. As described above, there is no reference in the specification for the elements 1110, 1130, 1140, and 1150: the load address match, load data match, and load flush, and load data. Therefore, these fields will be given a reasonable common English meaning. Also, the load attribute field is not defined explicitly and the same rule will be applied to it. As shown in figure 5, the extended load buffer holds a

load address. This address is updated as a result of a load instruction or an instruction that was matched as a load. Therefore, this field is also the load address match field. Figure 5 also shows that the table includes a PC field, which gives the age of the instruction. This is load data of a load instruction, which is also a load attribute. Since the data is written there upon realizing that an instruction matches a load instruction, the field is also a load data match. Column 9, lines 10-21 show that a load can be marked upon a match indicating that the load must be re-executed. Since the extended load buffer holds information for the loads, it is clear that this buffer would then hold the marking bits in such an embodiment as the prediction bits. Since the marking bits set above are marked not only on a match of addresses but also on improper ordering, these bits also signify a load flush because the load and subsequent instructions need to be flushed for re-execution as shown previously.

21. In regard to claim 8, Kahle in view of Yoaz has disclosed the apparatus of claim 1, as described above, wherein the CHT is one of indexed by a tag and tagless. Yoaz has shown in figure 2A a tagged CHT.

22. In regard to claim 9, Kahle in view of Yoaz has disclosed the apparatus of claim 1, as described above, wherein the CHT includes distance bits. Yoaz has shown in figure 2D a CHT including distance bits.

23. In regard to claim 10,

a. Kahle discloses an apparatus comprising:

i. a processor (figure 1) having internal memory (figure 1, element 1);

ii. a bus coupled to the processor (figure 1, element 2);

iii. a memory coupled to a memory controller and the processor; Column 2, line 65 – column 3, line 1 shows a memory used by and thus coupled to the processor. It is inherent that the memory has control logic so that it can be manipulated.

iv. an extended load buffer; Figure 5 gives a layout of a load queue which is also a buffer.

v. a marking unit coupled to the extended load buffer; Figure 6, shows in step 4 that a load program number is placed or marked into the load queue (extended load buffer). Therefore a marking unit must exist to perform this marking.

vi. a comparing unit coupled to the extended load buffer; Figure 6, step 6 and column 2, lines 56-59 show that a store address is compared to the load addresses of the load buffer. For this comparison to take place a comparison unit must exist.

vii. and a recovery unit coupled to the extended load buffer; Figure 6, steps 9 and 10 and column 3, lines 4-11 show that a load instruction must be placed in original order and reexecuted. It is shown that this is because of a conflict that exists and therefore original order must be recovered. This must be accomplished with a recovery unit.

viii. wherein unexecuted load instructions are advanced over store instructions. Column 2, lines 56-59 show that load instructions are executed out of order ahead of a store.

b. Kahle does not disclose a predictor having a collision history table (CHT) or that the extended load buffer is coupled to the predictor.

c. Yoaz has disclosed a predictor having a collision history table (CHT) (figure 3, element 88). Column 3, lines 50-52 show that the CHT is used for predicting and thus is part of a predictor along with the controller (figure 3, element 102). Figure 3 shows that the CHT or predictor is coupled to a recorder buffer, 94, using some control logic. Column 6, lines 35-36, shows that this buffer holds entries for load instructions. Yoaz has disclosed in column 3, lines 50-60 that the predictor is used for predicting load instructions so that loads can be executed ahead of stores.

d. Yoaz has shown in column 2, lines 58-63 that his method is able to execute more load instructions out of order (based on the predictor) for faster processor operations. These faster processor operations would have motivated one of ordinary skill in the art to modify the design of Kahle to use the collision history table and predictor described by Yoaz.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Kahle to include the predictor disclosed by Yoaz so that processor operations may be sped up.

24. In regard to claim 15, Kahle in view of Yoaz has disclosed the apparatus of claim 10, as described above, wherein the predictor is memory dependent. Column 3, lines 54-60 of Yoaz show that predictor is based on memory addresses and thus is memory dependant.

25. In regard to claim 16, Kahle in view of Yoaz has disclosed the apparatus of claim 10, wherein the extended load buffer comprises bit fields to mark load address match, load data match, load predict, and load flush, and bit fields for load address, load attribute and load data. As described above, there is no reference in the specification for the elements 1110, 1130, 1140, and 1150: the load address match, load data match, and load flush, and load data. Therefore, these fields will be given a reasonable common English meaning. Also, the load attribute field is not defined explicitly and the same rule will be applied to it. As shown in figure 5, the extended load buffer holds a load address. This address is updated as a result of a load instruction or an instruction that was matched as a load. Therefore, this field is also the load address match field. Figure 5 also shows that the table includes a PC field, which gives the age of the instruction. This is load data of a load instruction, which is also a load attribute. Since the data is written there upon realizing that an instruction matches a load instruction, the field is also a load data match. Column 9, lines 10-21 show that a load can be marked upon a match indicating that the load must be re-executed. Since the extended load buffer holds information for the loads, it is clear that this buffer would then hold the marking bits in such an embodiment as the prediction bits. Since the marking bits set above are marked not only on a match of addresses but also on improper ordering, these bits also signify a load flush because the load and subsequent instructions need to be flushed for re-execution as shown previously.

26. In regard to claim 17, Kahle in view of Yoaz has disclosed the apparatus of claim 10, as described above, wherein the CHT is one of indexed by a tag and tagless. Yoaz has shown in figure 2A a tagged CHT.

27. In regard to claim 18, Kahle in view of Yoaz has disclosed the apparatus of claim 10, as described above, wherein the CHT includes distance bits. Yoaz has shown in figure 2D a CHT including distance bits.

28. In regard to claim 19,

a. Kahle discloses a method comprising:

i. fetching an instruction (figure 6, step 1) and determining if an instruction is one of a store and a load (figure 6, step 3);

ii. executing the store instruction (figure 6, step 5);

iii. comparing an address and data of the store with load instructions in an extended load buffer (figure 6, steps 6 and 8); Figure 5 gives a layout of the load queue used in figure 6 to hold load information. This queue is also a buffer. The PC value indicates a program number for comparison of age of the instructions and thus is data of the instructions.

iv. setting marking bits in the extended load buffer if a match is found in the comparing; Column 9, lines 10-21 show that a load can be marked upon a match indicating that the load must be re-executed. Since the extended load buffer holds information for the loads, it is clear that this buffer would then hold the marking bits in such an embodiment.

v. updating a memory with store instruction if the store instruction can be retired; Column 6, lines 37-39 show that the memory is updated when the result of a store is committed or retired.

vi. and bypassing a silent store instruction and executing the load instruction if the instruction is a load. Column 2, lines 56-59 show that load instructions are executed out of order ahead of a store. Since load instructions can be advanced past any store, they will also be advanced past silent stores.

b. Kahle does not disclose performing a silent store prediction if the instruction is a store;

c. Lipasti discusses the notion of a silent store on page 183, column 2, last paragraph. It has the same definition as given by the applicant. Lipasti has shown on page 184, column 1, a set of prediction tables, each of which are store predictors. Further down in the column it is shown that one category of prediction is SameAddr/RightVal, or the store is to a same address and with a predicted value, so no changes will actually be made and thus a silent store is predicted.

d. Page 185, section 3.1 then shows that squashing these silent stores may allows a designer to obtain greater performance from existing structures, or a reduction in size or complexity of the system. This ability to obtain greater performance or reduction in size would have motivated one of ordinary skill in the

art to modify the design of Kahle to include the silent store prediction given by Lipasti.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Kahle to include the silent store prediction of Lipasti so that greater performance or size or complexity reduction can be realized.

29. In regard to claim 20, Kahle in view of Lipasti has disclosed the method of claim 19, as described above, further comprising preparing the load instruction for retirement, and marking the load instruction flush in the extended load buffer. Column 6, lines 20-24 of Kahle show that a load is committed or retired. In preparation for this, the address and program number are removed from the load queue. Since the marking bits set above are marked not only on a match of addresses but also on improper ordering, these bits also signify a load flush because the load and subsequent instructions need to be flushed for re-execution as shown previously.

30. In regard to claim 21,

a. Kahle in view of Lipasti has disclosed the method of claim 19, as shown above,

b. Kahle in view of Lipasti does not disclose wherein the predicting includes marking bits in a collision history table (CHT).

c. Yoaz has disclosed a wherein the predicting includes marking bits in a collision history table (CHT) (figure 3, element 88). Column 3, lines 50-52 show that the CHT is used for predicting. Column 5, lines 57-67, show updating or marking the CHT.

d. Yoaz has shown in column 2, lines 58-63 that his method is able to execute more load instructions out of order (based on the predictor) for faster processor operations. These faster processor operations would have motivated one of ordinary skill in the art to modify the design of Kahle in view of Lipasti to use the collision history table and predictor described by Yoaz.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Kahle in view of Lipasti to include the predictor disclosed by Yoaz so that processor operations may be sped up.

31. In regard to claim 22, Kahle in view of Lipasti discloses the method of claim 19, wherein the memory is a cache. As shown in column 6, lines 37-39 of Kahle, the completed store operation writes to a memory via a cache, thus the operation writes to the cache memory as well as a memory.

32. In regard to claim 23,

a. Kahle discloses a program storage device readable by a machine comprising instructions that cause the machine to:

i. fetch an operation (figure 6, step 1) and determining if an instruction is one of a store and a load (figure 6, step 3);

ii. execute the store instruction (figure 6, step 5);

iii. compare an address and data of the store operation with load operations in an extended load buffer (figure 6, steps 6 and 8); Figure 5 gives a layout of the load queue used in figure 6 to hold load information.

This queue is also a buffer. The PC value indicates a program number for comparison of age of the instructions and thus is data of the instructions.

iv. setting marking bits in the extended load buffer if a match is found in the compare instruction; Column 9, lines 10-21 show that a load can be marked upon a match indicating that the load must be re-executed. Since the extended load buffer holds information for the loads, it is clear that this buffer would then hold the marking bits in such an embodiment.

v. update a memory with store operation if the store operation can be retired; Column 6, lines 37-39 show that the memory is updated when the result of a store is committed or retired.

vi. and bypass a store instruction and execute the load instruction if the instruction is a load. Column 2, lines 56-59 show that load instructions are executed out of order ahead of a store. Since load instructions can be advanced past any store, they will also be advanced past silent stores.

b. Kahle does not disclose performing a silent store prediction if the instruction is a store;

c. Lipasti discusses the notion of a silent store on page 183, column 2, last paragraph. It has the same definition as given by the applicant. Lipasti has shown on page 184, column 1, a set of prediction tables, each of which are store predictors. Further down in the column it is shown that one category of prediction is SameAddr/RightVal, or the store is to a same address and with a

predicted value, so no changes will actually be made and thus a silent store is predicted.

d. Page 185, section 3.1 then shows that squashing these silent stores may allows a designer to obtain greater performance from existing structures, or a reduction in size or complexity of the system. This ability to obtain greater performance or reduction in size would have motivated one of ordinary skill in the art to modify the design of Kahle to include the silent store prediction given by Lipasti.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Kahle to include the silent store prediction of Lipasti so that greater performance or size or complexity reduction can be realized.

33. In regard to claim 24, Kahle in view of Lipasti has disclosed the method of claim 23, as described above, wherein the instructions further cause the machine to prepare the load operation for retirement, and mark a load operation flush in the extended load buffer. Column 6, lines 20-24 of Kahle show that a load is committed or retired. In preparation for this, the address and program number are removed from the load queue. Since the marking bits set above are marked not only on a match of addresses but also on improper ordering, these bits also signify a load flush because the load and subsequent instructions need to be flushed for re-execution as shown previously.

34. In regard to claim 25,

a. Kahle in view of Lipasti has disclosed the method of claim 23, as shown above,

b. Kahle in view of Lipasti does not disclose wherein the instruction that causes the machine to predict silent stores includes an instruction that causes the machine to mark bits in a collision history table (CHT).

c. Yoaz has disclosed a wherein the instruction that causes the machine to predict silent stores includes an instruction that causes the machine to mark bits in a collision history table (CHT) (figure 3, element 88). Column 3, lines 50-52 show that the CHT is used for predicting. Column 5, lines 57-67, show updating or marking the CHT.

d. Yoaz has shown in column 2, lines 58-63 that his method is able to execute more load instructions out of order (based on the predictor) for faster processor operations. These faster processor operations would have motivated one of ordinary skill in the art to modify the design of Kahle in view of Lipasti to use the collision history table and predictor described by Yoaz.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Kahle in view of Lipasti to include the predictor disclosed by Yoaz so that processor operations may be sped up.

35. In regard to claim 26, Kahle in view of Lipasti discloses the program storage device of claim 23, wherein the memory is a cache. As shown in column 6, lines 37-39 of Kahle, the completed store operation writes to a memory via a cache, thus the operation writes to the cache memory as well as a memory.

36. Claims 2-5 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle in view of Yoaz as applied to claims 1, 6, 8-10, 15, and 17-18 above, and further in view of Lipasti.

37. In regard to claim 2,

a. Kahle in view of Yoaz has disclosed the apparatus of claim 1, as described above.

b. Kahle in view of Yoaz has not disclosed wherein the predictor is a silent store predictor.

c. Lipasti discusses the notion of a silent store on page 183, column 2, last paragraph. It has the same definition as given by the applicant. Lipasti has shown on page 184, column 1, a set of prediction tables, each of which are store predictors. Further down in the column it is shown that one category of prediction is SameAddr/RightVal, or the store is to a same address and with a predicted value, so no changes will actually be made and thus a silent store is predicted.

d. Page 185, section 3.1 then shows that squashing these silent stores may allows a designer to obtain greater performance from existing structures, or a reduction in size or complexity of the system. This ability to obtain greater performance or reduction in size would have motivated one of ordinary skill in the art to modify the design of Kahle in view of Yoaz to include the silent store prediction given by Lipasti.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Kahle in view of Yoaz to include the silent store prediction of Lipasti so that greater performance or size or complexity reduction can be realized.

38. In regard to claim 3, Kahle in view of Yoaz and further in view of Lipasti has disclosed the apparatus of claim 2, as described above, wherein the silent store predictor uses path based indexing and the path is based on branches. Column 5, lines 9-23 of Yoaz shows how the CHT (the predictor) is used. This section shows that the sequence of instructions is based on the correct prediction of branches. As shown in column 4, lines 8-10, the tag of the CHT is the linear instruction pointer. Thus, the predictor is indexed based on the linear sequence of instructions that is used based on branches.

39. In regard to claim 4, Kahle in view of Yoaz and further in view of Lipasti has disclosed the apparatus of claim 3, wherein the silent store predictor is coupled with a state machine. Column 4, lines 43-45 of Yoaz show that the CHT includes prediction bits being either sticky or saturating counters. A saturating counter in itself is a state machine because it varies its state or value based on inputs.

40. In regard to claim 5, Kahle in view of Yoaz and further in view of Lipasti has disclosed the apparatus of claim 4, wherein the state machine is one of a 1-bit, 2-bit, and a sticky bit. Column 4, lines 43-45 of Yoaz show that the CHT includes prediction bits being either sticky or saturating counters.

41. In regard to claim 11,

a. Kahle in view of Yoaz has disclosed the apparatus of claim 10, as described above.

b. Kahle in view of Yoaz has not disclosed wherein the predictor is a silent store predictor.

c. Lipasti discusses the notion of a silent store on page 183, column 2, last paragraph. It has the same definition as given by the applicant. Lipasti has shown on page 184, column 1, a set of prediction tables, each of which are store predictors. Further down in the column it is shown that one category of prediction is SameAddr/RightVal, or the store is to a same address and with a predicted value, so no changes will actually be made and thus a silent store is predicted.

d. Page 185, section 3.1 then shows that squashing these silent stores may allows a designer to obtain greater performance from existing structures, or a reduction in size or complexity of the system. This ability to obtain greater performance or reduction in size would have motivated one of ordinary skill in the art to modify the design of Kahle in view of Yoaz to include the silent store prediction given by Lipasti.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Kahle in view of Yoaz to include the silent store prediction of Lipasti so that greater performance or size or complexity reduction can be realized.

42. In regard to claim 12, Kahle in view of Yoaz and further in view of Lipasti has disclosed the apparatus of claim 11, as described above, wherein the silent store

predictor uses path based indexing and the path is based on branches. Column 5, lines 9-23 of Yoaz shows how the CHT (the predictor) is used. This section shows that the sequence of instructions is based on the correct prediction of branches. As shown in column 4, lines 8-10, the tag of the CHT is the linear instruction pointer. Thus, the predictor is indexed based on the linear sequence of instructions that is used based on branches.

43. In regard to claim 13, Kahle in view of Yoaz and further in view of Lipasti has disclosed the apparatus of claim 12, wherein the silent store predictor is coupled with a state machine. Column 4, lines 43-45 of Yoaz show that the CHT includes prediction bits being either sticky or saturating counters. A saturating counter in itself is a state machine because it varies its state or value based on inputs.

44. In regard to claim 14, Kahle in view of Yoaz and further in view of Lipasti has disclosed the apparatus of claim 13, wherein the state machine is one of a 1-bit, 2-bit, and a sticky bit. Column 4, lines 43-45 of Yoaz show that the CHT includes prediction bits being either sticky or saturating counters.

Conclusion

45. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

46. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents and publications have been cited to further show the art with respect to load boosting and silent stores.

US Pat No 5,931,957 to Konigsburg shows a load buffer and comparing store information with loads in that buffer to se if out-of-order loads were speculated correctly.

US Pat No 6,058,472 to Panwar shows another method of load boosting by comparing stores to loads.

Characterizaion of Silent Stores by Lipasti shows extensive background and characterization of silent stores.

Silent Stores for Free by Lipasti shows a method for using load/store queues for forwarding when detecting silent stores.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

SFG
December 8, 2003

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